

### **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

#### **Listing of Claims:**

Claim 1 (Currently Amended): A digital-to-analog converting circuit comprising:

    a first potential terminal for supplying a first potential;  
    a second potential terminal for supplying a second potential;  
    an output node for outputting an analog signal;  
    a first resistor circuit having a plurality of first resistors connected in series between a first node and the output node through a plurality of first connecting points;

    a first switching circuit ~~having a plurality of~~ including P-channel type MOS transistors, each of the P-channel type MOS transistors ~~which is~~ connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only the P-channel type MOS transistors are connected to the first resistors as switches;

    a second resistor circuit having a plurality of second resistors connected in series between a second node and the output node through a plurality of second connecting points;

    a second switching circuit including ~~having a plurality of~~ N-channel type MOS transistors, each of the N-channel type MOS transistors ~~which is~~ connected directly to

the second potential terminal, and to respective ones of the second connecting points and the second node, wherein only the N-channel type MOS transistors are connected to the second resistors as switches; and

a control circuit connected to the first and second switching circuits for controlling the P-channel type MOS transistors and the N-channel type MOS transistors.

Claim 2 (Canceled)

Claim 3 (Previously Presented): A digital-to-analog converting circuit according to claim 1, wherein the second switching circuit further has an N-channel type MOS transistor connected between the second potential terminal and the output node.

Claim 4 (Canceled)

Claim 5 (Previously Presented): A digital-to-analog converting circuit according to claim 1, wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors and a second decoder for controlling the N-channel type MOS transistors.

Claim 6 (Original): A digital-to-analog converting circuit according to claim 1, wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 7 (Original): A digital-to-analog converting circuit according to claim 1, further comprising an amplifier connected to the output node for amplifying the analog signal.

Claim 8 (Currently Amended): A digital-to-analog converting circuit comprising:

a first potential terminal supplying a first potential;

a second potential terminal supplying a second potential;

an output node providing an analog signal;

a plurality of first resistors connected in series between a first node and the output node, the first resistors being connected to each other at a plurality of first connecting points;

a plurality of first switches P-channel type MOS transistors each of which is connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node, wherein only P-channel type MOS transistors are connected to the first resistors as switches;

a plurality of second resistors connected in series between a second node and the output node, the second resistors being connected to each other at a plurality of second connecting points;

a plurality of N-channel type MOS transistors second switches each of which is connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node, wherein only N-channel type MOS transistors are connected to the second resistors as switches; and

a control circuit connected to control the P-channel type MOS transistors and the N-channel type MOS transistors.

Claim 9 (Canceled)

Claim 10 (Previously Presented): A digital-to-analog converting circuit according to claim 8, further comprising an additional N-channel type MOS transistor connected between the second potential terminal and the output node.

Claim 11 (Canceled)

Claim 12 (Previously Presented): A digital-to-analog converting circuit according to claim 8, wherein the control circuit includes a first decoder for controlling the P-channel type MOS transistors and a second decoder for controlling the N-channel type MOS transistors.

Claim 13 (Original): A digital-to-analog converting circuit according to claim 8, wherein the first potential is a reference potential and the second potential is a ground potential.

Claim 14 (Original): A digital-to-analog converting circuit according to claim 8, further comprising an amplifier connected to the output node for amplifying the analog signal.

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Claims 15-21 (Canceled)